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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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LSI LOGIC CORPORATION
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EXAMINER

TRINH, MICHAEL MANH

ART UNIT PAPER NUMBER

2822

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/791,337

Applicant(s)

PRITCHARD ET AL.

Examiner

Michael Trinh

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 March 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2-15, 19-24 and 26 is/are pending in the application.
- 4a) Of the above claim(s) 2-15 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 19-24 and 26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☐ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application
- ☐ Other: _____

DETAILED ACTION

*** This office action is in response to Applicant's amendment and RCE filed March 03, 2007. Claims 2-15, 19-24, 26 are pending, in which claims 2-15 are non-elected, without traverse.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 112

1. Claim 26 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In claim 26, original specification and drawings do not support for the step of "...forming a strained silicon channel in the gate electrode trench after lining the trench with the high-K dielectric layer" and "...forming a conductive gate electrode in electrical contact with the strained silicon channel...".

As oppositely shown in Figure 2D, the strained silicon channel 204 is formed before the gate electrode and before lining the trench with the high-K dielectric layer. As shown in Figures 2E-2D, the high-K dielectric layer is thus formed before the strained silicon channel 204. Then, as shown in Figures 2F-2G, the gate electrode 208 is separated from the strained silicon channel with the high-K dielectric layer 202, and thus the gate electrode is not in electrical contact with the strained silicon channel.

Claim Rejections - 35 USC § 103

2. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sing et al (6,645,818) taken with Inumiya (6,054,355).

Sing teaches a method of forming a semiconductor integrated circuit, the method comprising: providing a substrate comprised of semiconductor material 10 having isolation structures 12 formed thereon, the substrate exposing the semiconductor material 16 having a planar surface located above the N-well region 16 so that the isolation structures 12 define exposed transistor forming regions of the substrate surface (Fig 1; col 2, lines 56-65); forming source and drain diffusion regions 34 in exposed transistor forming regions of the substrate

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surface (Fig 4; col 3, lines 13-17); annealing the semiconductor substrate (col 3, lines 18-24); after forming the source and drain diffusion regions 34 and after annealing, covering the surface of the semiconductor substrate with a first layer 76 (Fig 13; col 4, lines 45-52) of dielectric material to form a first interlayer dielectric layer 76 on the semiconductor substrate after formation of the source and drain diffusions 34; etching a gate electrode trench (Fig 13) in the interlayer dielectric layer 76 (col 4, lines 53-57), the gate electrode trench configured for the placement of a transistor gate electrode 84/86 between the source and drain regions 34; lining the gate electrode trench with a high-K dielectric film 82 (Fig 14; col 4, lines 58-65); and depositing a gate electrode 86/84 conductive material in the gate electrode trench after lining the trench with the high-K dielectric film 82 (Fig 14-15; col 4, line 58 through col 5).

Re claim 19, Sing already teaches providing the substrate 10 comprised of semiconductor material having isolation structures 12 (as shown in Figure 1). Claim 19 recites the substrate having a planarized surface.

Although, as shown in Figure 1 of Sing, the substrate 10 having isolation structures 12 appears to have a planar surface, Inumiya further teaches (at Figs 52B-58; col 36, line 30 through col 37; Figs 40A-40B; col 23, line 65 through col 24, line 8;) forming a substrate (61 in Fig 52B; 401 in Fig 40A) comprised of semiconductor material having isolation structures (62 in Fig 52B; 402 in Fig 40A), wherein the substrate 61,401 is formed to have a planarized surface by planarization (Fig 52B, 40A, col 24, lines 1-8).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the semiconductor device of Sing by providing the substrate having a planarized surface by planarization as taught by Inumiya. This is because of the desirability to increase the planarized surface area of the substrate so as to form a planarized semiconductor device, thereby forming a thinner and miniaturized planar semiconductor device.

Re claims 19-20, Sing does not teach forming a trench extension into the substrate (claim 19); and Re claim 20, the trench has a depth to include an entire device inversion channel.

However, Inumiya further teaches (at Figs 53-58, col 37, lines 20-42; Figs 60A-61B; col 41, lines 15-28; Figs 65A-65C, col 43, line 43 through col 44) etching the gate electrode trench in the first dielectric layer 66 to form a trench extension that extends into the substrate 61 (Figs 53B,54,,58,65A-65C), wherein the trench extension extends into the substrate a depth sufficient

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to include an entire device inversion channel for the integrated circuit device (as shown in Figs 53B, 54, 58, 65A-65C).

Therefore, it would have been also obvious to one of ordinary skill in the art at the time the invention was made to form the integrated circuit device of Sing by forming a trench extension that extends into the substrate to a depth sufficient to include an entire device inversion channel for the integrated circuit device, as taught by Inumiya. This is because of the desirability to bury the gate electrode in the trench recessed in the substrate thereby improving planarization of the semiconductor device, and because of the desirability to increase thickness of the gate electrode, thereby reducing wiring resistance, and thereby improving driving speed performance of the semiconductor device.

3. Claims 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sing et al (6,645,818) taken with Inumiya (6,054,355), as applied to claims 19-20 above, and further of Sugawara (6,750,486) and Hammond et al (6,680,496).

The references including Sing and Inumiya teach a method of forming a semiconductor integrated circuit as applied to claims 19-20 above.

Re claims 21-24, The references including Sing and Inumiya lack epitaxially growing a strained silicon layer formed on a SiGe layer in the trench.

However, Sugawara teaches (at Figs 2-4; 1; col 4, line 57 through col 6) epitaxially growing a Ge-containing layer including SiGe layer on the channel trench, and a silicon layer thereon. Hammond also teaches (at Figs 3A-3B; col 6, line 40 through col 7; col 10, lines 46-61) epitaxially growing a strained silicon layer formed on a SiGe layer or Ge layer grown in the channel.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Inumiya by epitaxially growing a strained silicon layer formed on a SiGe layer or Ge layer grown in the channel, as taught by Sugawara and Hammond. This is because to enhance high mobility electron or hole channel in strained device.

Response to Amendment

4. No prior art rejection is made against new claim 26, which new claim 26 is rejected above as containing subject matter which was not described in the specification.

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5. Applicant's remarks filed October 18, 2006 with respect to pending claims 19-24 have been considered but are moot in view of the new ground(s) of rejection.

Applicant remarked that "...Sing...require the formation of dummy gates 20 to facilitate self-aligned fabrication...".

In response, this is noted and found unconvincing. Although Sing requires the formation of dummy gates 20 in some steps, the combined references including at least Sing and Inumiya still prima facie obviously teaches the invention as claimed in claim 19. Moreover, as clearly shown in Figure 13, the interlayer dielectric (ILD) 76 is formed after forming the source and drain regions 34/44 in the N-well, and after the annealing step. Therefore, the rejections are outstanding and maintained.

The Examiner recognizes that references cannot be arbitrarily combined and that there must be some logical reason why skilled in the art would be motivated to make the proposed combination of references. In re Regel 188 USPQ 136 (CCPA 1975). However, there is no requirement that the motivation to make the combination be expressly articulated in one or more of the references; the teaching, suggestion or inference can be found not only in the references but also from knowledge generally available to one of ordinary skill in the art. Ashland Oil v. Delta Resins 227 USPQ 657 (CAFC 1985). The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin 170 USPQ 209 (CCPA 1971); In Re Rosselet 146 USPQ 183 (CCPA 196). References are evaluated by what they collectively suggest to one versed in the art, rather than by their specific disclosures. In Re Simon, 174 USPQ 114 (CCPA 1972); In Re Richman 165 USPQ 509, 514 (CCPA 1970).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The central fax phone number is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Michael Trinh
Primary Examiner